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## DESCRIPTION

MATCHED FILTER AND CORRELATION DETECTION METHOD

## 5 Technical Field

The present invention relates to a matched filter used for synchronization establishment processing in a spread spectrum communication system and a correlation detection method using the matched filter.

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## Background Art

In mobile communications, a spread spectrum communication with high frequency utilization efficiency capable of high-speed and high quality data communication, a CDMA (Code Division Multiple Access) system in particular, is becoming mainstream in recent years.

An area covered by one base station is called a "cell". If it is possible to increase the radius of a cell, the number of base stations can be reduced. Thus, the radius of a cell is an important factor in a mobile communication system and the radius of a cell may actually extend a few tens of km.

In the case where the radius of a cell reaches a few tens of km, the distance from a mobile unit to a base station varies a great deal when the mobile unit is close to the base station and when the mobile unit is located near the cell boundary. Therefore, the amount of delay of a signal received by the base station varies a great

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deal.

When a CDMA-based mobile communication between a mobile terminal apparatus and a base station starts, the base station needs to carry out high-speed initial  
5 synchronization processing taking into account a sufficiently large radius of a cell first.

For example, when the mobile terminal apparatus requests the base station, which is the communication target, for a communication permission, the base station  
10 learns how far the mobile terminal apparatus is located by measuring a propagation delay time relative to a reference signal.

That is, it is possible to know a rough distance to the mobile station by the base station sending a  
15 reference signal to the mobile station at a predetermined timing (reference timing) and measuring a time (this corresponding to a propagation delay time) required for an ACK (acknowledge signal) to be sent from the mobile station in response thereto. As a result, the base  
20 station can narrow the search range of correlation detection to a certain degree when detecting an acknowledge signal from the mobile station in response to the signal sent from the base station.

The propagation delay time is calculated with  
25 reference to delay profile information obtained by a matched filter circuit.

When creating a delay profile, the matched filter carries out a so-called data scan/code fixed despreading

calculation. That is, a spreading code necessary for a  
 despreading calculation of a target symbol is set  
 (code-fixed) in the matched filter and a correlation value  
 is calculated by inputting reception data continuously  
 5 over a search segment which is determined with a  
 propagation delay time taken into account.

FIG.21 shows a configuration of a conventional  
 matched filter.

Spreading codes generated by code generator 106 are  
 10 stored in code register 107. Code register 107 consists  
 of 256 shift registers 104b.

Then, reception data is input serially to shift  
 register 105. Every time 1-chip reception data is input,  
 despreading calculation section 109 multiplies the  
 15 parallel outputs of shift register 105 by the outputs  
 of code register 107. Despreading calculation section  
 109 consists of 256 multiplication circuits 108.

Then, integrating calculation segment 103 (provided  
 with integration circuit 110) integrates the parallel  
 20 outputs of despreading calculation section 109 and  
 calculates a correlation value corresponding to 1-symbol  
 data.

Suppose the search range (width of delay time) is  
 0 to 255 chips (equivalent to 1 symbol). Since the above  
 25 calculation is carried out every time data is shifted  
 by one chip, 256 calculations in total are required.

Since the matched filter detects a correlation on  
 a symbol-by-symbol basis, one matched filter can process

only a reception signal with a 1-symbol propagation delay.

Here, because of a large radius of a cell, if the search range (width of delay time) extends from 0 to 11 chips (equivalent to 2 symbols), one matched filter is not enough, and therefore two matched filters 904 and 906 are used as shown in FIG.22A.

The two matched filters 904 and 906 in FIG.22A operate at reference timings which are different from each other and both matched filters output a delay profile equivalent to one symbol.

FIG.22B is a timing chart to illustrate operations of the two matched filters.

As shown in the figure, matched filter 904 operates at a first reference timing and matched filter 906 operates at a second reference timing with a delay time equivalent to one symbol.

An operation of each matched filter will be explained taking processing of the first symbol as an example.

At time T1, a first symbol spreading code is set in matched filter 904 and a correlation calculation on the first symbol is performed while shifting the input data one chip at a time. A search from chip 0 to chip 255 (first-half search) finishes at time T2.

Then, at time T2 (second reference timing), a first symbol spreading code is set in matched filter 906 and a correlation calculation on the first symbol is performed while shifting the input data one chip at a time until time T3. A search from chip 256 to chip 511 (last-half

search) finishes at time T3.

At time T2, a second symbol detection code is set in matched filter 904 and a search on the second symbol starts.

5 By combining the search results from chip 0 to chip 255 and the search results from chip 256 to chip 511 on the first symbol calculated in this way together, it is possible to obtain a delay profile with a time equivalent to two symbols with respect to the first symbol.

10 However, the use of a plurality of matched filters will increase the scale of the circuit and extremely increase power consumption as well. That is, as the area occupied by the LSI chip increases, both costs and current consumption increase accordingly.

15 In reality, however, the radius of a cell (coverage) tends to necessarily be increased, which also causes propagation delays to increase, and covering those propagation delays needs to further increase the number of matched filters.

20 Moreover, mobile terminal apparatuses and base stations actually use a plurality of matched filters to generate and calculate delay profiles under various conditions. In this case, an increase of the scale of the circuit and increase of cost and power consumption  
25 constitute problems, too.

As shown above, since conventional matched filters have low processing performance, it is difficult to meet current demands by correlation detection using those

matched filters.

It is an object of the present invention to improve by far the efficiency (processing speed) of correlation detection processing using matched filters and thereby  
5 suppress increases of the scale of the circuit and solve the problems of power consumption.

That is, use of the present invention basically allows a single matched filter to even handle cases where a base station has a large radius of a cell or where mobile  
10 stations calculate delay profiles under multiple conditions.

#### Disclosure of Invention

The present invention does not perform fixed-code  
15 and data scanning type despreading calculations. Instead, the present invention performs fixed-data and code scanning type despreading calculations.

A fixed-data and code scanning type despreading calculation refers to a system to calculate correlation  
20 values by fixing reception data for a predetermined period and multiplying the fixed data by one spreading code after another according to respective propagation delays.

The reason that conventional matched filters have low processing performance of correlation calculations  
25 is that the speed (that is transfer rate of shift registers) at which reception data is input is low and this low speed constitutes constraints on the speed of the entire correlation detection processing. That is, the cause is

that the processing performance of the matched filter hardware is not fully exploited.

Thus, the present invention adopts a system of fixing reception data and scanning spreading codes. This  
5 eliminates constraints on the speed caused by inputting data to the matched filters.

On the other hand, the present invention can generate spreading codes and perform arithmetic calculations such as multiplications and additions incomparably faster than  
10 data transfers by shift registers. Thus, the processing performance of hardware determines the performance of correlation detection processing. Therefore, the present invention can exploit the potential capacity of hardware to the full and thereby allows efficient  
15 correlation calculation processing unparalleled among conventional arts.

Therefore, the present invention, using a single filter, can achieve completely the same result of generating delay profiles through data scan/code-fixed  
20 type despreading calculations using a plurality of matched filters. For example, when used to establish initial synchronization of a base station, the present invention can even handle, using a single matched filter, a case where a propagation delay from a mobile station  
25 is longer than a period equivalent to one symbol.

However, when input data is fixed as in the case of the present invention, not all the one-symbol data (256-chip data) may be constructed of data that belongs

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to one symbol. That is, immediately preceding symbol data bit is likely to be mixed with the current symbol data bit. A correlation value is obtained by integrating despread results with respect to one symbol, whereas  
5 integrating among partial despread results with respect to different symbols cannot obtain any correlation value. Therefore, it is necessary to strictly distinguish an integration calculation with respect to the immediately preceding symbol from an  
10 integration calculation with respect to the current symbol and handle these calculations separately.

Therefore, the present invention always needs to change integration calculation segments according to symbol segments. That is, data obtained through one  
15 despread process is divided into two segments in accordance with the position of a boundary between the immediately preceding symbol and the current symbol, an integration calculation is performed between the despread results with respect to the immediately  
20 preceding symbol and an integration calculation is performed between the despread results with respect to the current symbol. More specifically, every time a despread code is shifted by one chip, the end point (and start point) of the integration range is also shifted  
25 by one chip and the corresponding integration range is changed as appropriate.

Data obtained by each integration calculation is only a partial integration result. The integration



result (partial integration result) with respect to the current symbol is temporarily stored in memory. On the other hand, the data of the integration result (partial integration result) with respect to the immediately preceding symbol is added to the data of the partial integration result stored in memory during the previous correlation calculation processing, and in this way a correlation value on the immediately preceding symbol is obtained.

Furthermore, the data of the partial integration result with respect to the current symbol stored in memory is added to the data of the partial integration result calculated in the next correlation detection processing, and a correlation value is obtained at that time.

One preferred embodiment of the calculation method of the matched filter of the present invention carries out despreading by retaining and fixing input data in a temporary storage circuit and scanning spreading codes. With regard to the despreading result data obtained, this embodiment makes a distinction between a segment before a symbol delimiter (first-half symbol segment) which is uniquely determined according to the amount of phase shift of a spreading code and a segment after the symbol delimiter (last-half symbol segment) and integrates the despreading results with respect to the respective segments. Then, with respect to the first-half symbol segment, this integration result is added to the integration result corresponding to the same amount of phase shift of the

spreading code with respect to the same symbol retained as the result of the same processing as the previous processing. On the other hand, the integration result of the last-half symbol segment is temporarily stored and added to the integration result corresponding to the same amount of phase shift of the spreading code with respect to the same symbol obtained as the result of executing the next same processing, and correlations are thereby detected on a symbol-by-symbol basis. Then, a comparison is made between the detected symbol-by-symbol correlation values, a maximum correlation is detected and an actual amount of delay of the input data is thereby detected.

Another preferred embodiment of the calculation method of the matched filter of the present invention provides a temporary storage circuit that stores input data, a despreading calculation circuit that multiplies the input data temporarily stored in the storage circuit by spreading codes while scanning one chip at a time, an integration circuit that integrates despreading results with respect to a segment before a symbol delimiter (first-half symbol segment) which is uniquely determined according to the amount of phase shift of a spreading code and a segment after the symbol delimiter (last-half symbol segment), a storage circuit that temporarily stores the integration result of the last-half symbol segment, and an addition circuit that adds the integration result with respect to the first-half symbol segment to

the integration result corresponding to the same amount of phase shift of a spreading code with respect to the same symbol retained in the storage circuit as a result of the same processing as the previous processing and  
5 outputs a correlation value on one symbol.

The matched filter of the present invention can be used to detect correlations of spread spectrum modulated signals received by a base station and mobile stations. The present invention can easily extend a corresponding  
10 radius of a cell of a base station system and carry out delay profile calculations under various conditions using a circuit with a by far smaller scale than conventional arts. Furthermore, by installing a correlation detection circuit that incorporates the matched filter  
15 calculation circuit of the present invention in a mobile communication system such as a base station and mobile terminal apparatuses, it is possible to implement a mobile communication system at low costs and low power consumption as a result of an improved calculation method  
20 and calculation speed.

#### Brief Description of Drawings

FIG.1A illustrates a conventional code-fixed/data scan type correlation detection method;

25 FIG.1B illustrates features of a calculation (code scan/data-fixed system) according to a matched filter of the present invention;

FIG.2 illustrates a specific relationship between

an amount of delay of reception data, a spreading code and integration segment in a calculation (code scan/data-fixed system) according to the matched filter of the present invention;

5        FIG.3 illustrates a process until a correlation value is calculated in a calculation (code scan/data-fixed system) according to the matched filter of the present invention;

FIG.4 is a flow chart illustrating a characteristic  
10        processing procedure of a calculation method according to the matched filter of the present invention;

FIG.5 illustrates a method of proceeding with a calculation through data fixing/code scanning according to the matched filter of the present invention;

15        FIG.6 illustrates a basic concept of a calculation through data fixing/code scanning according to the matched filter;

FIG.7 illustrates a code scanning content of the matched filter of the present invention;

20        FIG.8 is a block diagram showing a basic configuration of the matched filter that carries out a calculation through data fixing/code scanning according to the present invention;

FIG.9 illustrates an outline of an operation of an  
25        integration segment selection circuit of the matched filter in FIG.8;

FIG.10 is a block diagram showing a configuration of a CDMA receiver incorporating the matched filter of

the present invention;

FIG.11 is a block diagram of a matched filter according to Embodiment 1 of the present invention;

FIG.12 is a timing chart showing an operation of  
5 the matched filter in FIG.11;

FIG.13 is a block diagram of a matched filter according to Embodiment 2 of the present invention;

FIG.14 is a timing chart showing an operation of the matched filter in FIG.13;

10 FIG.15 is a block diagram of a matched filter according to Embodiment 3 of the present invention;

FIG.16 is a timing chart showing an operation of the matched filter in FIG.15;

FIG.17 is a block diagram of a matched filter  
15 according to Embodiment 4 of the present invention;

FIG.18 is a timing chart showing an operation of the matched filter in FIG.17;

FIG.19 is a block diagram of a matched filter according to Embodiment 5 of the present invention;

20 FIG.20 is a timing chart showing an operation of the matched filter in FIG.19;

FIG.21 is a block diagram showing a basic configuration of a conventional matched filter;

FIG.22A is a block diagram showing a conventional  
25 configuration for carrying out correlation detection using two matched filters; and

FIG.22B is a timing chart illustrating an outline of an operation of the conventional configuration shown

in FIG.22A.

#### Best Mode for Carrying out the Invention

Before explaining specific embodiments, a basic  
5 concept of the present invention will be explained below  
with reference to FIG.1 to FIG.7.

According to the conventional system, a spreading  
code is fixed and data is scanned as shown in FIG.1A.  
In contrast to this, the present invention adopts a system  
10 in which data is fixed and spreading codes are scanned  
one chip at a time as shown in FIG.1B.

As shown in FIG.1B, input data is divided into  
processing periods  $T_n$  corresponding to a 1-symbol period  
( $=T_s$ ), latched and fixed in a shift register in this unit.  
15 In the figure, processing segment  $T_1$  corresponds to the  
current period,  $T_0$  corresponds to a past processing period  
and  $T_2$  corresponds to a future processing period.

A processing period ( $T_n$ ) and symbol period ( $T_s$ ) are  
concepts independent of each other and not synchronized.  
20 That is, the symbol period ( $T_s$ ) is a period that exactly  
corresponds to one symbol of an actual reception signal,  
while the processing period ( $T_n$ ) is a division to execute  
processing which corresponds to the length of data latched  
into a shift register and is determined for convenience'  
25 sake to execute processing.

Thus, for example, processing period  $T_1$  includes  
a mixture of part of symbol ( $n-1$ ) and part of symbol ( $n$ ).  
In FIG.1B, the area in which this mixture of data exists

is enclosed by dotted line and indicated with code DS1.

It is not known how two neighboring symbols are mixed during one processing period.

Thus, assuming all possible cases where there might  
 5 be boundaries between symbols (delimiters between symbols), an integration (integration with respect to part of one symbol) is performed with symbols taken into account by shifting integration segments in the respective cases. Then, later all integration results  
 10 are combined together, correlation values with respect to one entire symbol are calculated, and these correlation values are compared to find a correlation peak. The timing that gives the correlation peak is the input timing of the actual reception data.

15 Here, a delimiter of symbols is uniquely (automatically) determined according to a delay corresponding to a number of chips by scanning spreading codes while shifting spreading codes from an initial state (a reference timing) one chip at a time. In FIG.1, an  
 20 actual delimiter of a symbol during processing period T1 is expressed with a heavy line.

As illustrated in the figure, if this symbol  
 delimiter is taken into account, during processing period T1, integration value (partial integration value) b of  
 25 the despreading result with respect to the data that belongs to symbol (n-1) and integration value (partial integration value) c of the despreading result with respect to the data that belongs to symbol (n) are obtained.

Integration value b of the desreading result with respect to the data that belongs to symbol (n-1) is added to integration value a (this "a" is an integration value corresponding to the amount of delay of the same reception  
5 signal) of the desreading result with respect to the data that belongs to symbol (n-1) which is calculated by processing one cycle ahead and stored in memory 10.

This allows a correlation value corresponding to an amount of delay with respect to symbol (n-1) to be  
10 calculated.

Integration value c of the desreading result with respect to the data that belongs to symbol (n) is stored in memory 12.

Then, this integration value c is added to  
15 integration value d (this "d" is an integration value corresponding to the amount of delay of the same reception signal) of the desreading result with respect to the data that belongs to symbol (n) which is calculated in the next processing cycle. This allows a correlation  
20 value corresponding to an amount of delay on symbol (n) to be calculated.

In this way, a correlation value (a value estimated to be a correlation value) on one symbol is calculated for every one chip and a correlation value peak (symbol  
25 timing) on the symbol is actually detected by detecting a maximum value from among those correlation values.

FIG.2A shows a specific example.

Suppose a case where there is no delay of reception



data (A to I) with respect to a reference signal of a base station, a case where there is a one-chip delay and a case where there is a two-chip delay. In all cases, data is latched into a shift register segmented by  
 5 processing period (current processing period) T0.

If there is no delay, data to be latched is "D, E and F" and in this case, the processing period and the symbol segment (symbol period) match.

On the other hand, in the case of the 1-chip delay,  
 10 data to be latched is "C, D and E" and the symbol delimiter is located between data C and data D.

On the other hand, in the case of the 2-chip delay, data to be latched is "B, C and D" and the symbol delimiter is located between data C and data D.

15 The latched data (one of DEF, CDE or BCD) is multiplied by a spreading code (despreading code) while shifting the spreading code one chip at a time.

First, a spreading code that corresponds to the case of no delay is multiplied. The spreading code in this  
 20 case is "o, p, q". The segment over which the results of multiplying the reception data elements by these spreading code chips are integrated is TS1 (which matches the processing period).

The next code to be multiplied is "n, o, p". The  
 25 segment over which the results of multiplying the reception data elements by these spreading code chips are integrated is divided into TS2 and TS3 taking into account the symbol segmentation.

The next code to be multiplied is "m, n, o". The segment over which the results of multiplying the reception data elements by these spreading code chips are integrated is divided into TS4 and TS5 taking into account the symbol delimiter.

The above-described processing is shown in the upper part of FIG.3. As shown in the lower part of FIG.3, in the cases of the 1-chip delay and the 2-chip delay, integration values (b, c) obtained through partial integration are each added to integration value a corresponding to the same delay calculated in the immediately preceding cycle or integration value d corresponding to the same delay calculated in the next cycle. This makes it possible to obtain symbol-unit correlation values (values estimated to be correlation values) S0 to S4. S0 is a 1-symbol correlation value with no delay, S1 and S2 are partial correlation values of neighboring symbols in the case of the 1-chip delay, and S3 and S4 are partial correlation values of neighboring symbols in the case of the 2-chip delay.

Then, these symbol-unit correlation values S0 to S4 are compared.

As shown at the bottom of FIG.3, in the case of the 1-chip delay, correlation peaks are detected. Therefore, it is found that the latched reception data had a 1-chip delay. That is, it is understood from FIG.2 that the latched reception data were "D, E, F". With this, the timing of processing the reception signal has been

detected.

According to the above-described method, since the input data is fixed, the limit to the speed at which data is input to the shift register (reception data transfer rate) has no problem. Moreover, since this method performs multiplications repeatedly by shifting spreading codes 1 chip at a time over a period corresponding to a propagation delay covered by the base station, it is possible to perform processing at the maximum speed of hardware. Therefore, even if the search time width (propagation delay) to calculate a correlation value exceeds a time corresponding to 1 symbol, a single matched filter is enough to handle this.

The characteristic operations described above can be summarized as shown in FIG.4.

That is, data corresponding to a processing period is extracted and stored in memory of the matched filter (step 20).

Despreading is performed while shifting the phase 1 chip at a time, then the integration period is sequentially changed according to the number of chips of the code that has been shifted and the despreading results are integrated (step 21).

Then, when it is assumed that there is no delay of the reception signal relative to the reference timing of the base station (step 22), the value of integration of the despreading results itself becomes a correlation value with respect to 1 symbol (step 23).

On the other hand, in step 22 when it is assumed that there is a delay of the reception signal, data elements of different symbols are mixed in one data segment, and therefore the integration result with respect to the first-half symbol is added to the already calculated past (corresponding to the same delay) integration result to detect the correlation with respect to the symbol. On the other hand, for the last-half symbol, the integration result thereof is temporarily stored in memory. The stored integration result is added to the integration result with respect to part of the corresponding symbol which is calculated in the next cycle and the correlation with respect to the symbol is detected (step 24).

Then, a peak value is calculated by comparing correlation values of the respective symbols and the amount of actual delay of the reception data is detected (step 25).

This is the basic concept of data-fixed/code scanning type correlation detection of the present invention.

FIG.5 illustrates a relative positional relationship between the processing period and symbol delimiter of the reception signal when the search width is set to a time equivalent to 2 symbols. Each processing period ( $T_1$  to  $T_{n+2}$ ) is a time width equivalent to 1 symbol.

FIG.6 is an enlarged view of part of FIG.4.  $A_n(T)$  and  $B_n(T)$  in the figure indicate partial integration values of the despreading result.

In all cases of the  $(n-1)$ th processing period  $(T_{n-1})$ ,  
 $n$ th processing period  $(T_n)$  and  $(n+1)$ th processing period  
 $(T_{n+1})$ , the relative positional relationship between  
symbol delimiters  $P_1$ ,  $P_2$  and  $P_3$  and the start points and  
5 end points of the processing periods  $(t_{n-2}, t_{n-1}, t_n,$   
 $t_{n+1})$  is the same. In FIG. 6, one processing period (e.g.,  
 $T_n$ ) is divided into two segments by a symbol delimiter  
(e.g.,  $P_2$ ). The length of each part of the divided period  
is the same for the reception signal with the same amount  
10 of propagation delay for any processing period.  
Therefore, there will be no problem in each processing  
period, even if despreading and integration are performed  
and a partial integration value is calculated for each  
segment of the divided period independently of each other  
15 and then these partial integration values are added to  
the partial integration values to be calculated in the  
next processing period. Based on such a concept, the  
present invention performs partial integration  
processing for every processing period and adds up the  
20 partial integration values at the time of the next  
processing.

Here, the following discussion will be focused on  
a case where a propagation delay is " $T$ ".

During processing period  $T_{n-1}$ , partial integration  
25 value  $B_{n-1}(T)$  is calculated and stored in memory (not  
shown).

Then, in next processing period  $T_n$ , partial  
integration values  $A_n(T)$  and  $B_n(T)$  are calculated and

An(T) is added to partial integration value Bn-1(T) read from memory. A 1-symbol correlation value is calculated in this way. Bn(T) is stored in memory and added to partial integration value An+1(T) calculated in the next  
 5 processing to calculate a 1-symbol correlation value.

Thus, a delay profile obtained by the data-fixed/code scan system of the present invention is completely the same as that obtained by the conventional data scan/code-fixed system.

10 Here, spreading codes generated when calculations are performed for correlation detection by the data-fixed/code scan system of the present invention will be explained using FIG.7.

As shown in the figure, reception signal DA(n) to  
 15 DA(n+255) with a propagation delay of 0 chips is multiplied by spreading code CO(n) to CO(n+255). Likewise, reception signal DA(n-1) to DA(n+254) with a propagation delay of 1 chip is multiplied by spreading code CO(n-1) to CO(n+254).

20 Here, if attention is focused on a change of the spreading code caused by a change of the amount of propagation delay of the reception signal, it is observed that every time the propagation delay is incremented by 1 chip, the spreading code is shifted 1 chip backward.

25 Therefore, using the spreading code with a propagation delay of 0 chips as an initial value, spreading codes are generated one after another with their respective contents shifted one chip at a time. These

sequentially generated spreading codes are multiplied on fixed data.

With reference now to the attached drawings, embodiments of the present invention will be explained  
5 below.

(Embodiment 1)

FIG.8 shows a basic configuration example of a matched filter of the present invention.

Matched filter circuit 201 of the present invention  
10 includes data register 202 that receives reception data serially and outputs data in parallel, despreading calculation section 203, integration calculation section 204 and code generator 206 that generates spreading codes (despreading codes).

15 Data register 202 is fed reception data serially. Then, when 1-symbol data corresponding to one processing period ( $T_n$ ) is stored as explained using FIG.5 and FIG.6, data register 202 outputs the reception data in parallel. That is, data register 202 functions as a serial/parallel  
20 conversion circuit.

The data output in parallel from data register 202 is latched into data register 205.

Code generator 206 includes a recursive shift register constructed by combining exclusive OR circuits  
25 214 and 215, and shift register 213. This recursive shift register is a generator of M series spreading codes. This code generator 206 generates spreading codes which are shifted 1 chip at a time. In this embodiment, code

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generator 206 outputs spreading codes each corresponding to 1 symbol (= 256 chips) in parallel.

The 256-bit spreading codes generated from this code generator 206 are stored in code register 207.

5        Spreading circuit 208 multiplies the 1-symbol equivalent reception data output in parallel from data register 205 by spreading codes output in parallel from code register 207.

10       Integration calculation section 204 includes integration segment selection circuit 209, integration circuit 210, memory 211 and addition circuit 212.

Integration segment selection circuit 209 receives data bits indicating a despreading calculation result of 256 bits output from despreading circuit 208 in parallel.

15       The integration segment selection circuit divides the 256-bit data into two segments at an arbitrary position and can output only data bits of one group in parallel. That is, the integration segment selection circuit can select data bits to be sent to integration circuit 210

20       from among the 256-bit data. This realizes partial integration in each processing period explained in FIG.6. More specifically, integration segment selection circuit 209 automatically changes from one integration segment to another in association with a supposed amount of delay

25       of the reception data. The delimiting point between integration segments (position at which 256-bit data is divided into two segments) is a position (P1, P2, P3 in FIG.6) which could always serve as a delimiter for 1 symbol

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as shown in FIG.6.

Integration circuit 10 executes an integration calculation, which gives partial integration values ( $A_n(T)$  and  $B_n(T)$  if the current processing period is  $T_n$ ) shown in FIG.6.

One of the partial integration values (e.g.,  $B_n(T)$  in FIG.6) is written to memory 211. Memory 211 has an address space equivalent to a propagation delay. The other partial integration value output from integration circuit 210 (e.g.,  $A_n(T)$  in FIG.6) is added by addition circuit 212 to the partial integration value obtained in the previous processing (e.g.,  $B_{n-1}(T)$  in FIG.6) read from memory 211. This gives a correlation value with respect to 1 symbol.

The correlation value (correlation output) obtained is temporarily stored in memory 215.

Then, peak detection circuit 216 compares among the stored correlation values and find a correlation peak. An amount of delay of the reception data is determined according to this correlation peak. In this way, the timing for processing the reception signal is detected (FIG.3).

FIG.9 illustrates an operation of integration segment selection circuit 209.

As described above, integration segment selection circuit 209 automatically changes from one integration segment to another in association with a supposed amount of delay of the reception data. The delimiting point

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between integration segments (position at which 256-bit data is divided into two segments) is a position (P1, P2, P3 in FIG.6) which could always serve as a delimiter for 1 symbol in the actual reception data as explained in FIG.6.

Thus, as shown in FIG.8, over a range of propagation delay of 0 chips to 1 chip of the reception signal, the 256-bit data is divided into two segments at symbol delimiter P1 and in this way the integration period is automatically determined. Likewise, over a range of propagation delay of 1 chip to 2 chips, the integration period is determined according to symbol delimiter P2 and over a range of propagation delay of 2 chips to 2.5 chips, the integration period is determined according to symbol delimiter P3.

In this way, integration segments are changed one after another by integration period selection circuit 209 according to symbol segments of the reception signal.

## 20 (Embodiment 2)

FIG.10 is a block diagram showing a main configuration of a CDMA reception apparatus incorporating the matched filter of the present invention.

This receiver includes reception antenna 401, high frequency signal processing section 402 that carries out predetermined filtering and amplification, A/D converter 403, demodulator 409, decoder 410, CODEC section 411 that converts a decoded signal to voice, matched filter 404,

clock generator 407 and PLL circuit 408.

A reception signal subjected to spectrum spreading is converted from serial to parallel at data register 405 of matched filter 404, stored and fixed in a data register of correlation calculation section 406.

Matched filter 404 can multiply fixed data by codes at high speed based on a high-speed clock signal supplied from PLL circuit 408. Thus, matched filter 404 implements extremely high-speed despreading calculation processing.

This allows the CDMA reception apparatus equipped with the matched filter of the present invention to carry out data-fixed/code scanning calculations at high speed and thereby allows single matched filter 404 to even handle a case where the search range required by the system exceeds a 1-symbol time. Thus, using the CDMA reception apparatus of the present invention makes it possible to easily extend the radius of a cell of the base station.

Furthermore, since the matched filter of the present invention can carry out calculations extremely fast, delay profile calculations under different conditions can be performed, for example, on a time-division basis. That is, the matched filter of the present invention is capable of performing high-level processing faster with smaller hardware. With this, it is possible to implement a high-function cellular phone with low power consumption.

(Embodiment 3)



In the matched filter in FIG.11, adder 307 adds up all despreading results corresponding to 1 symbol during one processing period (e.g.,  $T_n$  in FIG.6) ( $A_n(T) + B_n(T)$  in FIG.6).

5 Furthermore, integration segment selection circuit 304 partially integrates the data ( $B_n(T)$  in FIG.6) of the segment after a symbol delimiter ( $P_2$  in FIG.6).

Then, calculator 308 subtracts the output of adder 305 ( $B_n(T)$  in FIG.6) from the output of adder 307 ( $A_n(T) + B_n(T)$  in FIG.6). On the other hand, calculator 308 writes the output of adder 305 ( $B_n(T)$ ) to memory 306 and at the same time reads a partial integration value ( $B_{n-1}(T)$  in FIG.6) calculated by the immediately preceding processing from memory 306.

15 Then, adder 309 adds up a partial integration value ( $B_{n-1}(T)$  in FIG.6) output from memory 306 and the output of adder 308 ( $A_n(T)$  in FIG.6). This gives a correlation value on 1 symbol ( $B_{n-1}(T) + A_n(T)$  in FIG.6).

Then, more specific operations of data register 202, 20 despreading calculation section 203 and integration calculation section 302 in FIG.11 will be explained.

FIG.12 is a timing chart showing an operation of a calculation circuit of the matched filter of Embodiment 1 of the present invention. A to D described in FIG.12 25 represent signals A to D in FIG.11.

Data register 202 is always fed reception data serially.

First, a DATALOAD signal is validated at time  $T_1$ ,

and the content of data register 202 is taken into despreading calculation section 203 at time T2 synchronized with the clock signal.

At time t2, a spreading code to despread a reception  
 5 symbol which is a calculation target and arrives with a propagation delay of 0 is stored in despreading calculation section 203 and a despreading calculation is performed.

Furthermore, at same time T2, adder 307 adds up all  
 10 outputs of despreading calculation section 203 and outputs the addition result as C2(0) in FIG.12.

Furthermore, at same time T2, a DIV signal given to decoding circuit 303 becomes "0" and as a result, all bits of a 256-bit DECDIV signal are fixed at a high level  
 15 and these are given to integration segment selection circuit 304.

Since all bits of the DECDIV signal are fixed at a high level, integration segment selection circuit 304 fixes all the outputs at a low level. Adder 305 outputs  
 20 "0" as B2(0) in FIG.12.

At the same timing, value "0" is read as B1(0) during the immediately preceding processing period from the address indicated by an ADDRESS signal of memory 306.

Immediately after this, B2(0) is written at the same  
 25 address of memory 306.

As a result, calculator 308 outputs a value obtained by subtracting B2(0) from C2(0), that is, A2(0) and adder 309 adds up B1(0) read from memory 306 and output A2(0)

of adder 309 and outputs as correlation calculation result D2(0) in FIG.12.

The calculation contents from time T3 onward are repetitions of the above-described contents.

5        A DIV signal from time T2 to time T4 changes in connection with a supposed propagation delay of a reception target symbol and "0" to "255" are repeated.

DECDIV1 to DECDIV255 in FIG.12 vary periodically based on the DIV signal with patterns shown in FIG.12.

10       Furthermore, memory 306 includes a data storage area corresponding to the supposed propagation delay of a reception target symbol. The area to be accessed is changed according to a propagation delay of a reception signal.

15       Since the WRITE and READ signals in FIG.12 can perform a read and write operations according to a same clock to/from memory 306, memory 306 is always active during calculations.

20       The timing chart in FIG.12 shows an example where a delay profile of a 511-chip equivalent search width is generated during one 256-chip processing period. By increasing the clock rate used for calculation processing, it is possible to handle larger search widths.

25       Thus, the calculation circuit of the matched filter of this embodiment can output correlation calculation results according to a data-fixed/code scan system for every one clock.

(Embodiment 4)

FIG.13 is a block diagram showing a configuration of another embodiment of a matched filter of the present invention.

The function and operation of the matched filter of this embodiment are the same as those of the matched filter in FIG.11. However, in this embodiment, a cumulative addition of spread data is carried out in advance. This makes it possible to construct an integration segment selection circuit with a selector, which can simplify the circuit.

Matched filter circuit 501 in FIG.13 includes data register 202, code generator 206, despreading calculation section 203 and integration calculation section 502.

Integration calculation section 502 includes cumulative addition section 503, integration segment selection circuit 505, memory 306 and calculators 506 and 507.

Cumulative addition section 503 includes a plurality of addition elements 504a to 505e. The plurality of addition elements 504a to 505e has a function of cumulatively adding 256-bit data output from despreading calculation section 203 sequentially starting from the least significant bit. In FIG.13, b1 to b255 each denote data indicating cumulative addition results.

Integration segment selection circuit 505 selects any one (data B in the figure) of the data indicating the 255 cumulative addition results output from



cumulative addition section 503. Data B is written to memory 306 and sent to calculator 506 as well.

The result (data C in the figure) of an addition of all data bits indicating despreding results is  
 5 obtained from adder 505e. Calculator 506 carries out a calculation of  $(C-B)$ , and as a result obtains data A. This data A is added to the data read from memory 306, giving correlation output D.

Data is read from despreding calculation section  
 10 203 based on a DATALOAD signal. An integration segment of integration segment selection circuit 505 is specified based on a DIV signal.

Data register 202, code generator 206, despreding calculation section 203, memory 306, calculator 506 and  
 15 adder 507 are the same as those of the foregoing embodiments, and therefore explanations thereof will be omitted.

FIG.14 is a timing chart showing an operation of the matched filter shown in FIG.13.

First, a DATALOAD signal is validated at time T1,  
 20 and the content of data register 202 is taken into despreding calculation section 203 at time T2 synchronized with the clock signal.

Furthermore, at same time T2, adder block 503 cumulatively adds up outputs of the respective taps of  
 25 despreding calculation section 203 one after another and outputs b2 to b255 as the addition results of the respective taps as C2(0) in FIG.14.

At same time T2, a DIV signal becomes "0" and as

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a result, the DIV signal is output as B2(0) in FIG.14 from integration segment selection circuit 505.

At the same timing, data "0" acquired from memory 306 at the immediately preceding processing is read as B1(0) in FIG.14.

As a result, calculator 506 outputs a value obtained by subtracting B2(0) from C2(0), that is, A2(0). Then, adder 507 adds up B1(0) read from memory 306 and output A2(0) of adder 309 to obtain correlation calculation result D2(0) in FIG.14.

The calculation contents from time T3 onward are repetitions of the above-described contents.

Thus, the matched filter of this embodiment can output data fixed/code scanning correlation calculation results for every one clock. Furthermore, the matched filter of this embodiment can construct an integration segment selection circuit with a selector, which simplifies the circuit.

(Embodiment 5)

FIG.15 is a block diagram showing a configuration of another example of a matched filter of the present invention.

The basic function and operation of the matched filter of this embodiment are the same as those of the foregoing embodiments. However, this embodiment processes two pieces of reception data alternately using one integration segment selection circuit on a time-division basis. When the number of available

circuits is smaller than the number of signals to be processed, this configuration is suited to a case where one circuit is shared.

As opposed to the foregoing embodiments where a correlation value is output once for every one clock, in this embodiment, a correlation value with respect to one reception signal is output once for every two clocks.

In this embodiment, the signal input to the matched filter is a signal obtained by placing two types of reception signal data for one chip after another alternately and combining the two signals. That is, if the two types of signals are Q and W, the input signals are placed for one chip after another alternately such as Q1, W1, Q2, W2 ... It is possible to select a signal whose correlation value should be calculated by changing the cycle of a MASKEN signal.

This matched filter circuit 601 includes data register 202, code generator 206, despreading calculation section 203 and integration calculation section 602.

Integration calculation section 602 includes integration segment selection circuit 304, decoder section 303, adder 305, register 603, calculator 605 that subtracts the data value output from register 603 from the addition result of adder 305, memory 604 and adder 606 that adds up the output of calculator 605 and the data read from memory 604.

Data is read from despreading calculation section 203 based on a DATALOAD signal. An integration segment

of integration segment selection circuit 304 is specified based on a DECDIV signal and MASKEN signal output from decoder section 303. The content of the DECDIV signal output from decoder section 303 is determined based on  
 5 a DIV signal.

A read from memory 604 is carried out according to a clock different from that of a write to memory 604.

FIG.16 is a timing chart showing an operation of the matched filter in FIG.15.

10 Data register 202 is always fed reception data serially.

A DATALOAD signal is validated at time T1, and the data retained in data register 202 is taken into despreading calculation section 203 at time T2  
 15 synchronized with the clock signal.

At time T2, a spreading code to despread the reception symbol to be calculated with a propagation delay of "0" is set in despreading calculation section 203, a despreading calculation is performed and the result  
 20 is retained until time T4.

At same time T2, a DIV signal to decoding circuit 303 becomes "0" and a MASKEN signal to be given to integration segment selection circuit 203 is invalidated. This causes the output of despreading calculation section  
 25 203 to pass through integration segment selection circuit 203 and output as is.

As a result, the output of adder 305 becomes equivalent to the sum total of all the output bits of

despreading calculation section 203. This is data C2(0) in FIG.16.

Then, at time T3, C2(0) is written to register 603.

At time T3, the MASKEN signal is validated.

5 Furthermore, at time T2, the DIV signal drives all bits of the DECDIV signal to a high level. This causes all the output of integration segment selection circuit 304 to be fixed at a low level.

The addition result of adder 305 becomes "0". This  
10 addition result is B2(0) in FIG.16.

Calculator 605 outputs result A2(0) obtained by subtracting B2(0) from C2(0).

At time T2, a READ signal is validated. Then, at time T3, data B1(0) is output from memory 604.

15 Adder 606 outputs correlation calculation result D2(0) which is a sum of A2(0) and B1(0).

At time T4, data C2(0) is written at the same address of memory 604.

The calculation contents from time T4 onward are  
20 repetitions of the contents described above.

The DIV signal from time T2 to time T6 has the same function as that described in the foregoing embodiments, but is different from the foregoing embodiments in that it has 2 clock cycles.

25 DECDIV1 to DECDIV255 change periodically with patterns shown in FIG.16 based on the DIV signal.

The matched filter according to this embodiment can output a data-fixed/code scan type correlation

calculation result every two clocks. Moreover, use of the integration segment selection circuit on a time-division basis makes it possible to exploit limited hardware resources to the full to process many signals.

5 (Embodiment 6)

FIG.17 is a block diagram showing a configuration of another example of a matched filter of the present invention.

10 The function of the matched filter of this embodiment is the same as that of the matched filter in FIG.15. That is, the matched filter uses the integration segment selection circuit on a time-division basis and outputs a correlation value every two clocks.

15 However, as opposed to the embodiment in FIG.15 which controls an integration segment of integration segment selection circuit 304 using decoder 303, this embodiment controls the integration segment of integration segment selection circuit 304 using shift register 704. This simplifies the circuit configuration.

20 Shift register 704 is given an initial value signal generated by initial value generator 703, a LOAD signal and SHIFTEN signal.

More specific operations of initial value generator 703 and shift register 704 will be explained using FIG.18.

25 Data register 202 is always fed reception data serially.

First, a DATALOAD signal is validated at time T1, and the data retained in data register 202 is taken into

despreading calculation section 203 at time T2  
synchronized with the clock signal.

At time T2, a spreading code to despread the  
reception symbol to be calculated with a propagation delay  
of "0" is stored in despreading calculation section 203,  
5 a despreading calculation is performed and the result  
is retained until time T4.

At time T1, the LOAD signal is validated. At time  
T2 synchronized with the clock signal, an initial value  
10 generated by initial value generator 703 is taken into  
shift register section 704.

At time T2, the SHIFTEN signal is invalidated. This  
causes the shift operation of shift register 704 to stop  
at time T3.

15 Likewise, at time T2, a MASKEN signal input to  
integration segment selection circuit 304 is invalidated.  
This causes the completely the same data that is output  
from despreading calculation section 203 to be output  
from integration segment selection circuit 304.

20 At time T3, the SHIFTEN signal is validated. At  
time T4 synchronized with the clock, the shift operation  
of the shift register is validated. In this way, a shift  
operation is implemented once every two clocks.

Thus, this embodiment uses a shift register circuit  
25 instead of a decoder circuit that controls the integration  
segment selection circuit, and can thereby simplify the  
control circuit of the integration segment selection  
circuit. The function of the matched filter implemented

is the same as that of the matched filter in FIG.15.  
(Embodiment 7)

FIG.19 is a block diagram showing another example  
of a matched filter of the present invention.

5       The function of the matched filter of this embodiment  
is the same as that of the matched filter in FIG.17.  
However, since the matched filter in FIG.17 subtracts  
integration result B specified by shift register 704 from  
integration value C of all bits subjected to despreading  
10       calculations to calculate integration result A in order  
to calculate correlation calculation result D, this  
matched filter has a rather complicated circuit  
configuration.

Thus, this embodiment provides inversion control  
15       circuit 803 that inverts the output of shift register  
704 that selects an integration segment, partially  
inverts the output bit of shift register 704 and thereby  
calculates integration value A in an early stage. This  
makes it possible to reduce adders and memories, etc.  
20       considerably and simplify the circuit.

As is apparent from FIG.19, provision of inversion  
control circuit 803 causes the final stage circuit that  
calculates correlation values to be constituted only by  
memory 306 and adder 309, which simplifies the circuit  
25       configuration.

The integration segment of integration segment  
selection circuit 304 is determined by the output of  
inversion control circuit 803. Output data of inversion



control circuit 803 is obtained by inverting the output bit of shift register 704 based on an INV signal.

A more specific operation of inversion control circuit 803 will be explained using FIG.20.

5        Data register 202 is always fed reception data serially.

First, a DATALOAD signal is validated at time T1, and the data retained in data register 202 is taken into despreading calculation section 203 at time T2  
10        synchronized with the clock signal.

At time T2, a spreading code to despread the reception symbol to be calculated with a propagation delay of "0" is set in despreading calculation section 203, a despreading calculation is performed and the result  
15        is retained until time T4.

A LOAD signal is validated at time T1, and the output data of initial value generator 703 is taken into shift register section 704 at time T2 synchronized with the clock signal.

20        The SHIFTEN signal invalidated at time T2 invalidates the shift operation of shift register 704 at time T3.

At time T2, the level of the INV signal input to inversion control circuit 803 is fixed at a low level.  
25        This causes the data with all bits being "1" output from shift register 704 to be directly given to integration segment selection circuit 203. Integration segment selection circuit 203 outputs the same data bits as the

FIG. 20

output bits of all taps of despreding calculation section 203. Adder 305 adds up these data bits. This addition result is  $A2(0)$  in FIG.20.

At time  $T3$ , the INV signal is fixed at a high level. This causes the all "1" signals output from shift register 704 to be inverted for all bits and become all "0" data bits. These all "0" signals are given to integration segment selection circuit 304 and to integration segment selection circuit 304 outputs data with the values of all data bits of despreding calculation section 203 masked and which are all at a low level (all "0" data). Adder 305 outputs "0" as  $B2(0)$  in FIG.20.

At time  $T3$ , data  $B1(0)$  is read from an address specified by an ADDRESS signal of memory 306.

As a result, adder 309 outputs correlation calculation result  $D2(0)$  which is a sum of  $A2(0)$  and  $B1(0)$ .

Then, at time  $T4$  in FIG.18, data  $B2(0)$  is written at the same address of memory 306.

The calculation contents from time  $T4$  onward are repetitions of the above-described contents.

Embodiment 5 calculates integration result A by subtracting integration result B specified by shift register 704 from integration value C of the processing segment subjected to a despreding calculation to obtain correlation calculation result D. In contrast to this, this embodiment inverts the output of shift register 704 that selects an integration segment and can thereby calculate integration value A, too.

In FIG. 20, DECDIV1 to DECDIV255 change periodically with patterns shown in FIG. 20 based on DIV.

As shown above, this embodiment can reduce the number of adders and storage circuits by providing an inversion control circuit that controls inversion/non-inversion of output of the shift register that controls the integration segment selection circuit.

The present invention has been explained so far based on various embodiments. The foregoing explanations assume that the present invention is mainly used for a CDMA communication base station, but the present invention is not limited to this. For example, the present invention is also easily applicable, for example, to a case where a correlation of a data string with a plurality of different types of code is detected on the mobile station side.

As explained above, the present invention can carry out a data-fixed/code scan type correlation calculation, and therefore can speed up delay profile calculations more easily than prior arts. That is, the present invention eliminates constraints associated with the data input speed and allows calculation processing to be carried out 100% with the maximum processing performance of hardware that constitutes the matched filter.

As a result, the present invention can realize predetermined calculations with a matched filter of a smaller circuit scale. This allows a base station to easily extend the radius of a cell and a mobile station

(cellular phone) to carry out delay profile calculation processing on a time-division basis under different conditions. The present invention also allows a single matched filter to cover a propagation delay of 1 symbol or more. The present invention suppresses the scale of the circuit and can thereby reduce the space, thus making it possible to reduce the size of the LSI, hence the size of the system.

This application is based on the Japanese Patent Application No. 2000-099306 filed on March 31, 2000, entire content of which is expressly incorporated by reference herein.

#### Industrial Applicability

The present invention is applicable to a correlation detector (matched filter) in a CDMA receiver.